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Advantages and disadvantages of model order reductions

Signal processing

Introduction

High order linear phase finite response (FIR) filters are widely used in signal processing, because they allow distortion free transition of signals. Very high order may cause computational efforts. Therefore several model order reduction algorithms [1], [2], [3], [4] developed in control theory are adapted to order reduction of high order linear phase FIR filters. These algorithms relay on a similarity transformation [5] of an FIR filter. A similarity transformation brings an FIR filter into a balanced form. In [6] the advantages of balanced form were discussed. Namely, there were proved that every subsystem of balanced system is stable. Since order a reduced filter is indeed a subsystem of full order FIR filter, its stability is guaranteed. The stability of order reduced filters is interesting because of its infinite impulse response (IIR). Moreover the phase response is very linear particularly for pass-band frequencies. This is true for both analog and digital filters. In [7] we showed that order reduced digital filters can replace high order digital FIR filters in very complex ZePoC [8] structure where linear phase is desired. Here we will discuss whether order reduced digital filters can be used in low power applications, where their hardware implementation is required. Therefore we are interesting in difference between power consumption of hardware implemented FIR and order reduced IIR filters.

The paper is organized as follows. First we will describe power consumption of hardware elements used in digital filter structures. Then simulated distribution of power consumption of very high order FIR and order reduced IIR filters will be exhibited. The power consumed by several FIR and order reduced IIR filters will be compared and the paper will be concluded.

Power consumption of hardware blocks

Adders, multipliers and delay elements are hardware blocks in filter structures. Delay elements realized as flip-flops are very low power consumers. We consider ripple-carry

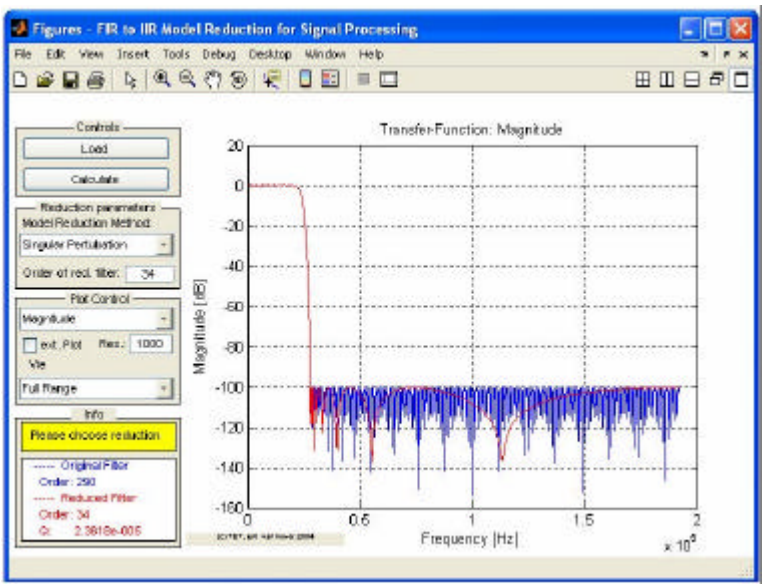

Figure 1: Graphic output of Matlab program for model order reduction of FIR filters

adders and Braun multipliers with constant coefficients realized by CMOS transistors. To describe power consumption of filter we have first to describe power consumption of CMOS inverter. Since inverter is power consumers only during loading and unloading of its gate load capacitance, the information about its switching activity is crucial. The transistor power consumption is a sum of its static and dynamic power components, where static power consumption is a consequence of the leakage and short-circuit currents [9] and it depends on the technology of used full-custom design. Since the same full custom design is used for FIR and order reduced IIR filters the static power consumption is similar for these two filters. On contrary the dynamic power consumption depends on the selected filter structure and may be represented as a sum of power consumption during capacitance reloading and the cross-flow current power consumption. In general we may assume that the power consumption that occurs because of the cross-flow current is 20% of the power consumption that occurs because of the capacity reloading [10]. Then the dynamic power consumption is

$$P_{dynamic} \sim \frac{1}{2} V_{DD}^2 \, f m_E C_E , \tag{1}$$

Where V_{DD} is supply voltage, f is a clock frequency, C_E is an equivalent gate load capacitance, while m_E is an activity of transistors that build equivalent capacitance C_E. Our approach is simple. We assumed that cascaded transistors may be represented by

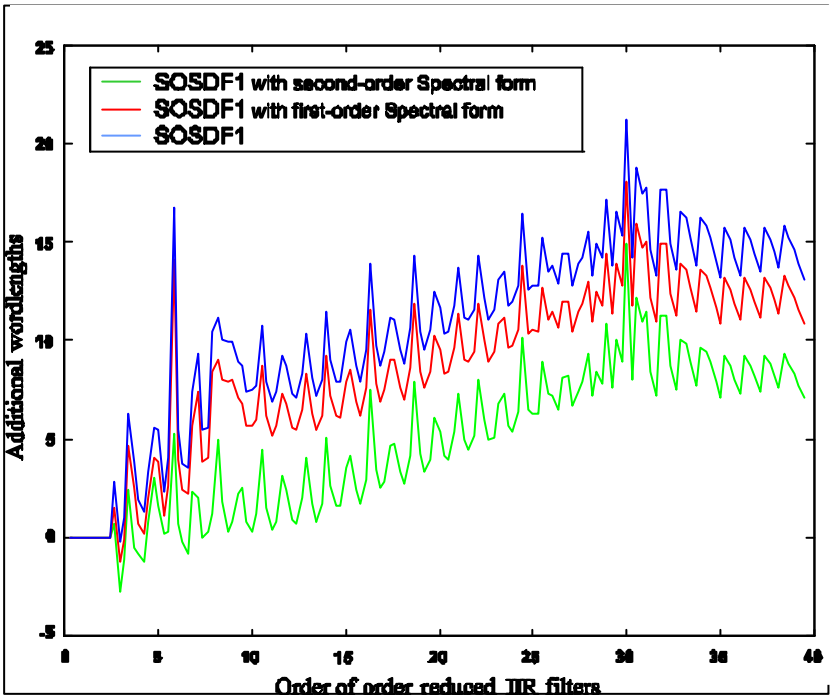

Figure 2: Additional bits necessary for equal quantization noise between FIR and order reduced IIR filters

equivalent capacitance, which is the sum if all gate load capacitance of transistors in cascade. The influence of connections between transistors was not included in calculations. Therefore equation (1) shows a simple description of filter power consumption. Since supply voltage, clock frequency and equivalent gate load capacitance are common for filters represented in the same full-custom technology, they do not participate to the difference between power consumption of FIR and order reduced IIR filters. Contrary the transistor activities m_{FIR} and m_{IIR} in FIR and IIR filter CMOS circuits, respectively, participate to the difference in the power consumption between the filters. This is because the transistor activity depends on the filter structure, i.e. total amount of used transistors. Indeed the difference between the power consumption of FIR and order reduced IIR filters is

$$D_{iff} \sim \frac{P_{dynamicFIR}}{P_{dynamicIIR}} = \frac{m_{FIR}}{m_{FIR}} . \tag{2}$$

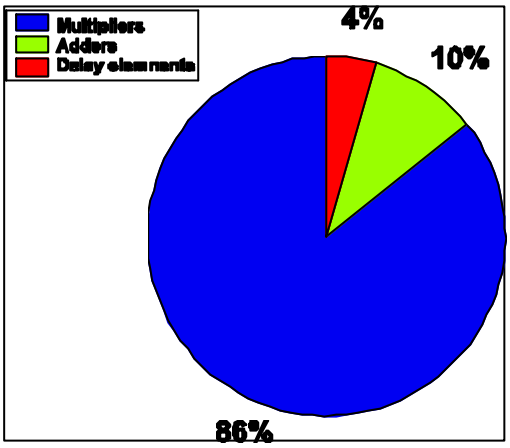

Figure 3: Power consumed by building elements of FIR filter

Power consumed by hardware implemented filters

To estimate power consumption of an arbitrary chosen FIR filter and order reduced IIR filter, we programmed simulator in MATLAB 7.0.1 version for Windows. The simulator contains several procedures.

First procedure starts with an FIR filter design using *sptool* function from *Signal Processing Toolbox*. The created FIR filter is loaded by option *Load* in the MATLAB program, see figure 1. The procedure selects the bound Hankel singular value of the FIR filter, which ordinal index indicates the order of order reduced filter. Choosing one of offered model order reduction technique and the option *Calculate*, the order reduced IIR filter is created. Moreover, the order of the reduced filter may be also arbitrary chosen, adding in the field *order of red. filter:* any number smaller that FIR filter order. In both cases the ideal arithmetic is used to obtain coefficients of order reduced filter. Using function *ss2sos* and ideal arithmetic the coefficients of cascaded second-order sections model are obtained. Since full-custom design uses only rounded and quantized coefficients, a representation of filter coefficients in two's complement 24 bit fixed-point arithmetic is ensured in the same program.

Next procedure that can be activated in the simulator, gives the number of additional bits necessary for the representation of order reduced IIR filter coefficients, so that quantization noise of order reduced IIR is equal to the quantization noise of an FIR filter. Orders of more than 15 the FIR filters are reduced and additional bits for order reduced IIR filters are calculated proceeding 500 samples long white noise. This white noise is used for all simulations. In figure 2 the additional word lengths for different recursive filter structures are

plotted. The results show that a recursive filter realized as cascaded second-order sections in direct form one (SOSDF1) with second-order spectral forms

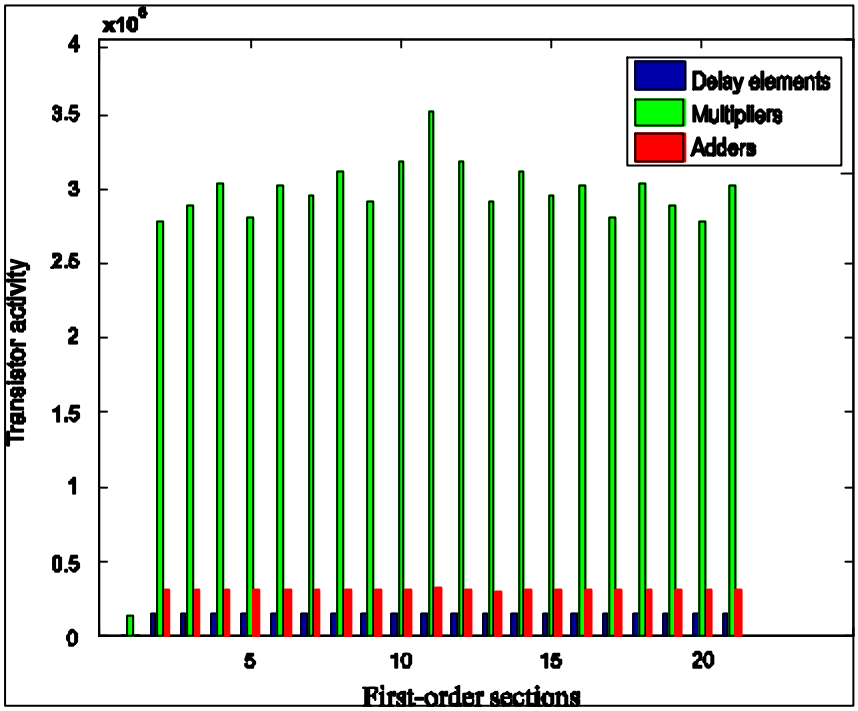

Figure 3 Power consumption of 20th order FIR filter

(SF) having the lowest quantization noise needs the lowest number of additional bits. The highest number of additional bits is required for cascaded second-order section without any spectral form. Moreover, the number of additional word length increases with filter order. Before we estimated power consumption of a filter implemented in a certain form, we simulated activity of multipliers, adders and delay elements in arbitrary chosen FIR filter. The result of simulation is exhibited in figure 3, which shows that multipliers are the main power consumers. Further the power consumption over filter structures is investigated. FIR filter realized in direct form can be divided on first-order sections. Each section contains one delay element, one adder and one multiplier. Power consumption calculated by using equation (1), and scaled by product of supply voltage, clock frequency and equivalent capacitance is function of only transistor activities. The estimated power consumption of several FIR filters realized in direct form shows uniform power distribution. In figure 4 the estimated power consumption of direct form FIR filter is exhibited. The FIR filter is divided on 20 first-order sections. Since the uniform distribution of power consumption is obtained, power distribution over an FIR filter may be obtained estimating power consumption of an arbitrary chosen first-order section and multiplying the result by the filter order. On this way estimated power consumption of an FIR filter realized in direct form is fast archived with

very small error. The error is assumed to be small, because a difference between transistor activities of two sections $\Delta \sim 2\times10^7$ is much smaller than transistor activities of one of sections 14×10^7, ($\Delta \ll 14\times10^7$, see figure 3).

If we reduce the order of this FIR filter, we obtain an IIR filter of order 10. The order

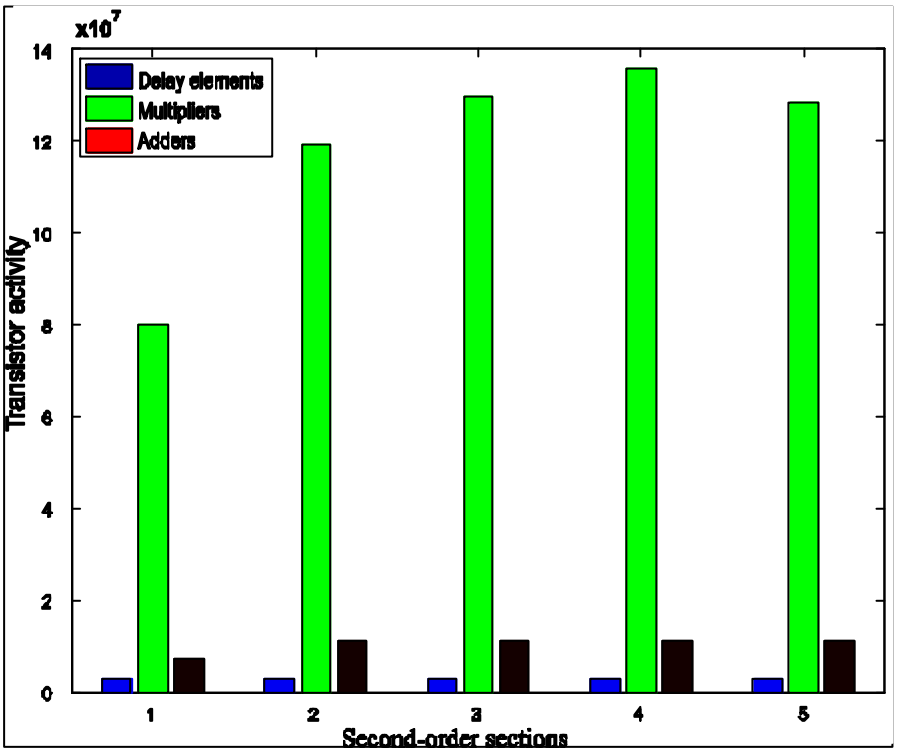

Figure 4: Power consumption of 10th order IIR filter

reduced IIR filter may be implemented as five cascaded second-order sections in direct form II. Distribution of estimated power consumption over second-order sections is plotted in figure 4. Very uniform distribution of estimated power consumption is obtained. Thus the total power consumption of an IIR filter realized as cascaded second-order section may be easily obtained estimating power consumption of an arbitrary selected second-order section and multiplying obtained power consumption by number of second-order sections. In this case error is also quite small because of small difference between consumed powers by second-order sections.

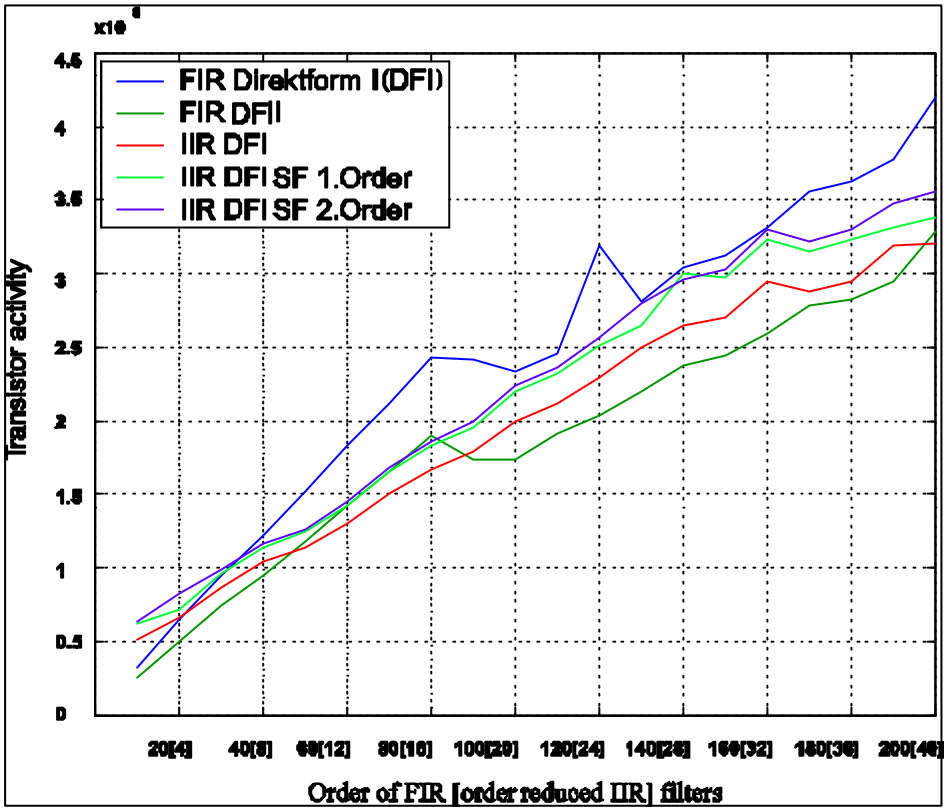

Figure 6: Power consumption of FIR and reduced IIR filters

To compare power consumption between FIR and order reduced IIR filters more than 10 linear phase FIR filters are reduced. Transistor activities of different realizations of transfer functions of FIR and order reduced IIR filters are simulated. Figure 6 shows that order reduced IIR filters are not always lower power consumers. Their power consumption depends on implementation form. Also FIR filters may exhibit lower power consumption than low order IIR filters. In this simulation the degree of order reduction for all filters is equal in order to eliminate its influence on results of simulation. Indeed, transistor activity depends on filter properties and implementation form.

Conclusions

In this paper we discussed an easy way to describe difference in power consumption between FIR and order reduced IIR filters. Describing power consumption of an arbitrary chosen filter implementation form by transistor activities during filtration of white noise, approximate results are obtained. With accepted error, uniform power distribution over FIR and order reduced IIR filters implementation forms is obtained. In order to obtain difference in power consumption between order reduced and FIR filters we simulated transistor activities of the most used filter structures.

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